09 683872 TRANSMITTAL LETTER Docket No. (General - Patent Issued) BUR920010100US1 adanza U.S. Patent No. **Issue Date** November 1, 2005 6,960,837 B2 METHOD OF CONNECTING COR I/O PINS TO BACKSIDE CHIP I/O PADS Title: **COMMISSIONER FOR PATENTS:** Transmitted herewith is: **Certificate of Correction** Postcard No fee is required below. Errors were made by the U.S. Patent Office. No additional fee is required. A check in the amount of is attached. The Director is hereby authorized to charge and credit Deposit Account 09-0456 (IBM) as described below. Charge the amount of \boxtimes Credit any overpayment. Charge any additional fee required. Payment by credit card. Form PTO-2038 is attached. WARNING: Information on this form may become public. Credit card information should not be

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Dated: 11-09-2005

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UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO.: 6,960,837 B2

DATED

: November 1, 2005

INVENTOR(S): Iadanza

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 7

Line 63, delete "black" and insert -- block--

Column 8

Line 47, delete "or" and insert -- of--

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